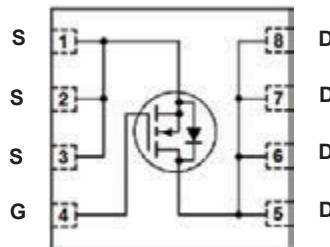
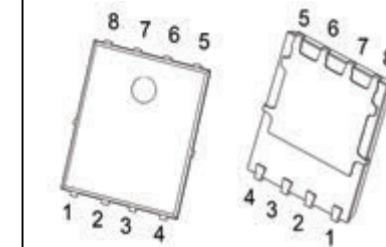


■ Features

- $V_{DS} = 100 \text{ V}$
- $I_D (\text{at } V_{GS}=10\text{V}) = 100 \text{ A}$
- $R_{DS(\text{ON})} (\text{at } V_{GS} = 10 \text{ V}) < 4.2 \text{ m}\Omega$
- $R_{DS(\text{ON})} (\text{at } V_{GS} = 4.5 \text{ V}) < 6.0 \text{ m}\Omega$
- 100% UIS Tested
- 100% R_g Tested



PDFN5x6-8(PDFNWB5x6-8L)

**■ Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)**

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	100	A
		100	
Pulsed Drain Current (Note 2)	I_{DM}	320	
Continuous Drain Current	I_{DSM}	30.5	
		24.5	
Avalanche Current (Note 2)	I_{AS}	65	A
Avalanche Energy $L = 0.1\text{mH}$ (Note 2)	E_{AS}	211	mJ
Thermal Resistance, Junction- to-Ambient (Note 5)	$R_{\theta JA}$	50	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction- to-Case	$R_{\theta JC}$	0.58	
Power Dissipation (Note 4)	P_D	215	W
		86	
Power Dissipation (Note 5)	P_{DSM}	6.2	
		4.0	
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to 150	

Notes:

1. The maximum current rating is package limited.
2. Single pulse width limited by junction temperature $T_J(\text{MAX})=150^\circ\text{C}$.
3. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
4. The power dissipation P_D is based on $T_J(\text{MAX})=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
5. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $TA = 25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA} t \leq 10\text{s}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.

■ Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$\text{Id} = 250 \mu\text{A}, \text{V}_{\text{GS}} = 0\text{V}$	100			V
Zero Gate Voltage Drain Current	Id_{SS}	$\text{V}_{\text{DS}} = 100 \text{V}, \text{V}_{\text{GS}} = 0 \text{V}$		1		μA
		$\text{V}_{\text{DS}} = 100 \text{V}, \text{V}_{\text{GS}} = 0 \text{V}, T_J = 55^\circ\text{C}$		5		
Gate to Source Leakage Current	I_{GSS}	$\text{V}_{\text{DS}} = 0 \text{V}, \text{V}_{\text{GS}} = \pm 20 \text{V}$		± 100		nA
Gate to Source Threshold Voltage	$\text{V}_{\text{GS(th)}}$	$\text{V}_{\text{DS}} = \text{V}_{\text{GS}}, \text{Id} = 250 \mu\text{A}$	2.3		4.3	V
Static Drain-Source On-Resistance	$\text{R}_{\text{DS(on)}}$	$\text{V}_{\text{GS}} = 10 \text{V}, \text{Id} = 20 \text{A}$		3.7	4.2	$\text{m}\Omega$
		$\text{V}_{\text{GS}} = 10 \text{V}, \text{Id} = 20 \text{A}, T_J = 125^\circ\text{C}$			6.8	
		$\text{V}_{\text{GS}} = 4.5 \text{V}, \text{Id} = 20 \text{A}$			6.0	
Forward Transconductance	g_{FS}	$\text{V}_{\text{DS}} = 5 \text{V}, \text{Id} = 20 \text{A}$		100		S
Dynamic Characteristics						
Input Capacitance	C_{iss}	$\text{V}_{\text{GS}} = 0 \text{V}, \text{V}_{\text{DS}} = 50 \text{V}, f = 1 \text{MHz}$		5940		pF
Output Capacitance	C_{oss}			1475		
Reverse Transfer Capacitance	C_{rss}			24		
Gate Resistance	R_g	$\text{V}_{\text{GS}}=0\text{V}, \text{V}_{\text{DS}}=0\text{V}, f = 1\text{MHz}$	0.3	0.6	1.0	Ω
Switching Characteristics						
Total Gate Charge (10V)	Q_g	$\text{V}_{\text{GS}} = 10 \text{V}, \text{V}_{\text{DS}} = 50 \text{V}, \text{Id} = 20 \text{A}$		80	115	nC
Total Gate Charge (4.5V)				35	50	
Gate Source Charge	Q_{gs}			18		
Gate Drain Charge	Q_{gd}			11		
Turn-On Delay Time	$t_{\text{d(on)}}$	$\text{V}_{\text{GS}} = 10 \text{V}, \text{V}_{\text{DS}} = 50 \text{V}, R_L = 2.5 \Omega, R_{\text{GEN}} = 3 \Omega$		16.5		ns
Turn-On Rise Time	t_r			6.5		
Turn-Off Delay Time	$t_{\text{d(off)}}$			46		
Turn-Off Fall Time	t_f			12		
Drain-Source Diode Characteristics						
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 20 \text{A}, dI/dt = 500 \text{ A}/\mu\text{s}$		43		ns
Body Diode Reverse Recovery Charge	Q_{rr}			207		
Maximum Body-Diode Continuous Current	I_S	(Note 1)			100	A
Diode Forward Voltage	V_{SD}	$\text{V}_{\text{GS}} = 0 \text{V}, I_S = 1 \text{A}$		0.68	1	V

Notes:

6. The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.
7. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_J(\text{MAX})=150^\circ\text{C}$. The SOA curve provides a single pulse rating.
8. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$.

SMD Type

MOSFET

■ Typical Electrical and Thermal Characteristics

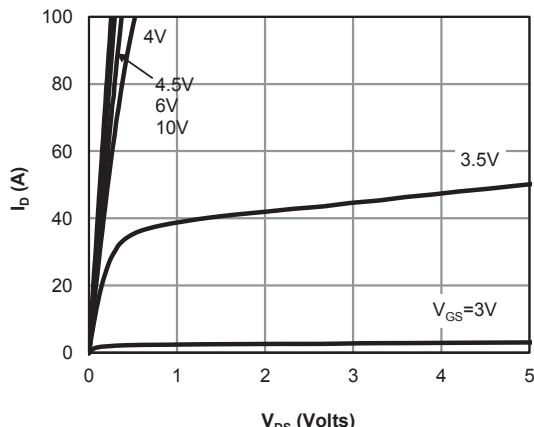


Figure 1: On-Region Characteristics (NOTE 6)

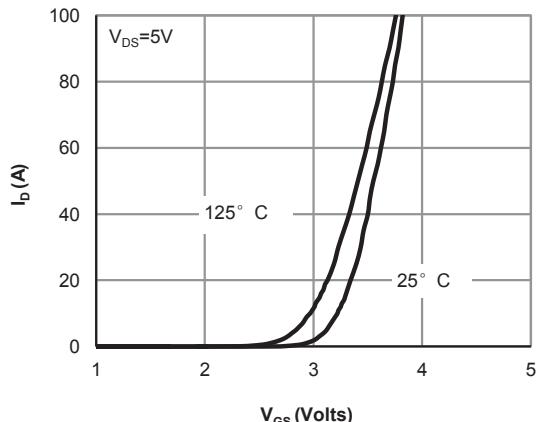


Figure 2: Transfer Characteristics (NOTE 6)

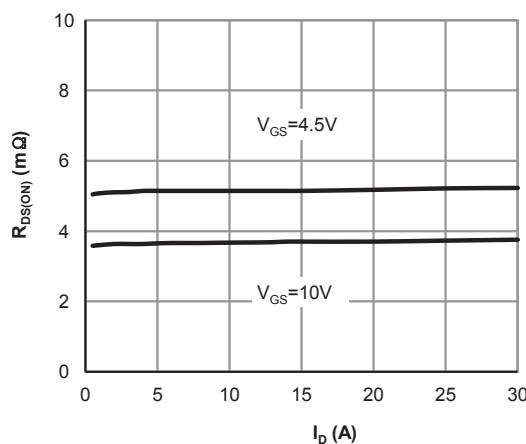
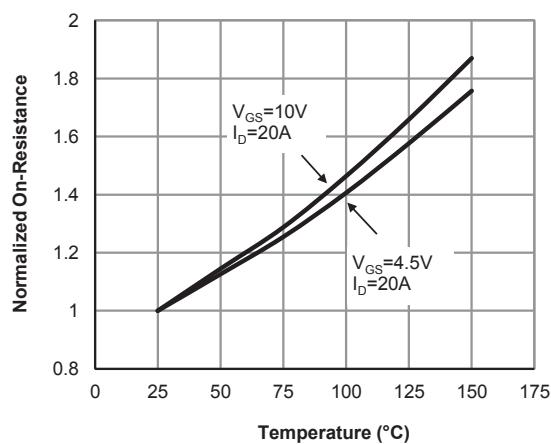
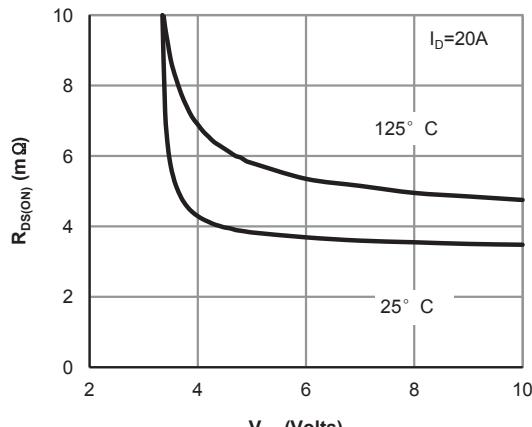


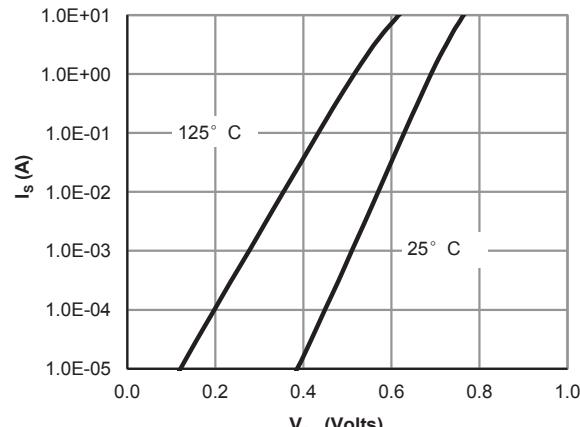
Figure 3: On-Resistance vs. Drain Current and Gate Voltage (NOTE 6)



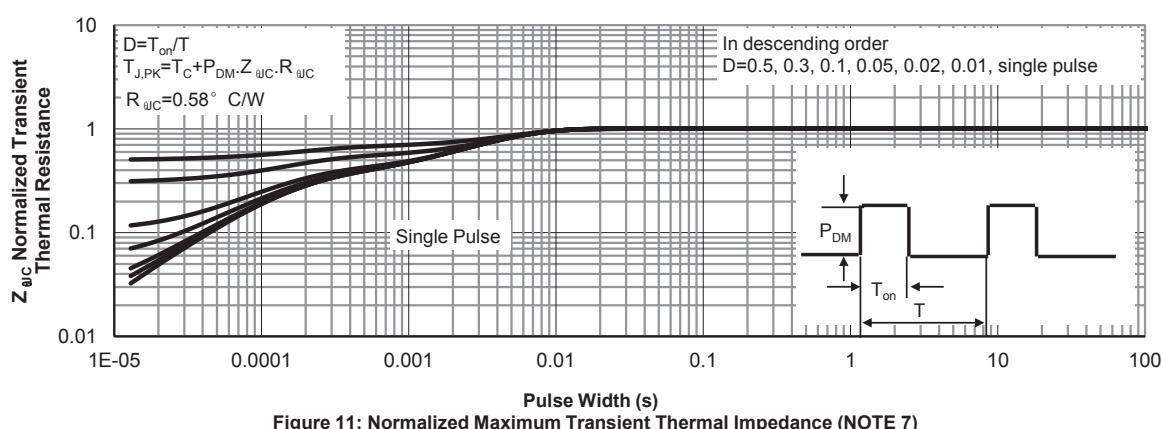
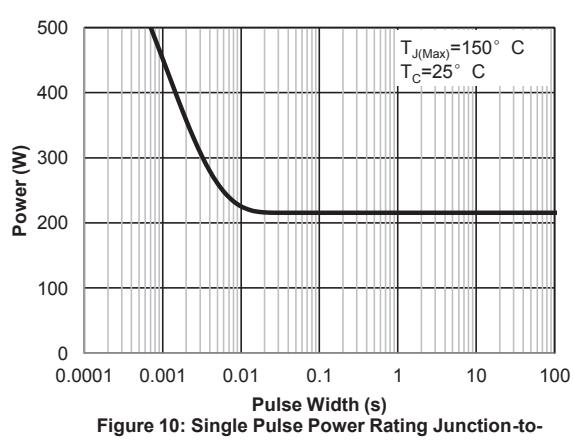
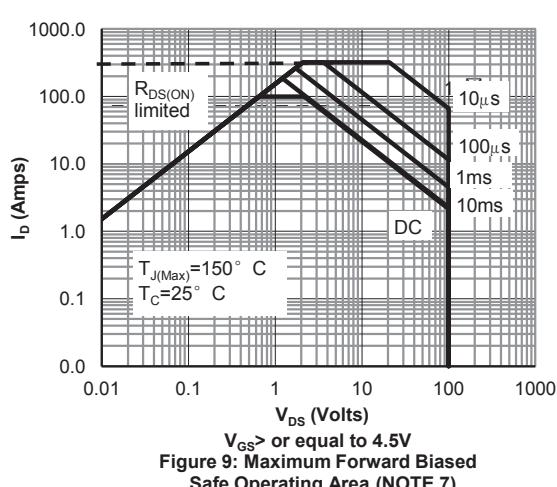
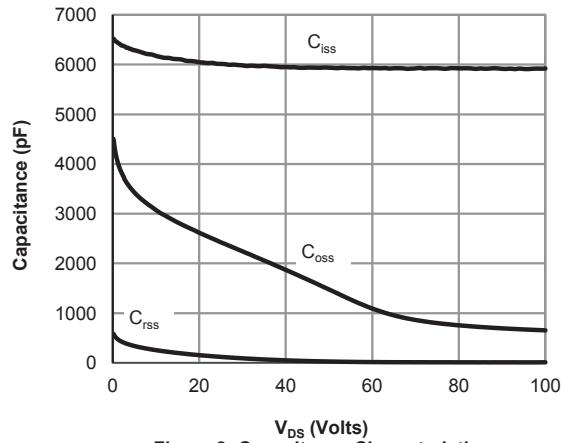
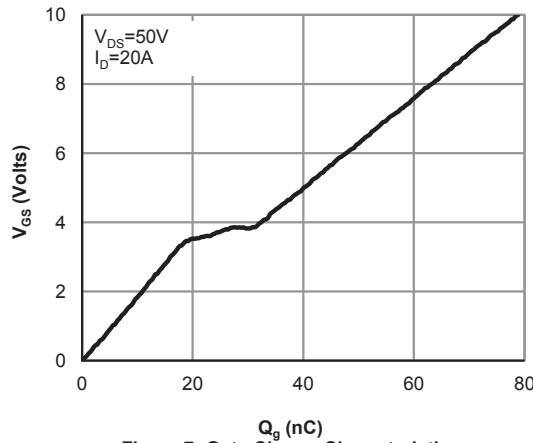
**Figure 4: On-Resistance vs. Junction Temperature
(NOTE 6)**



**Figure 5: On-Resistance vs. Gate-Source Voltage
(NOTE 6)**



**Figure 6: Body-Diode Characteristics
(NOTE 6)**



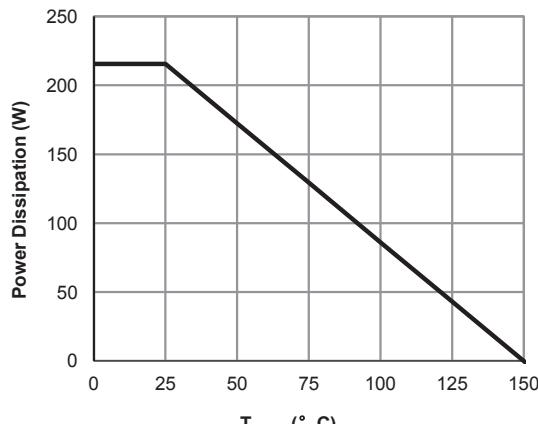


Figure 12: Power De-rating (NOTE 7)

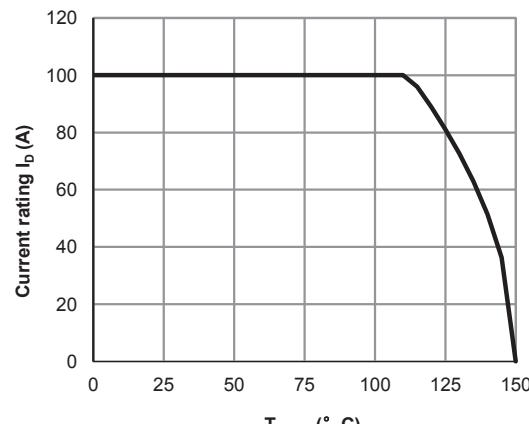


Figure 13: Current De-rating (NOTE 7)

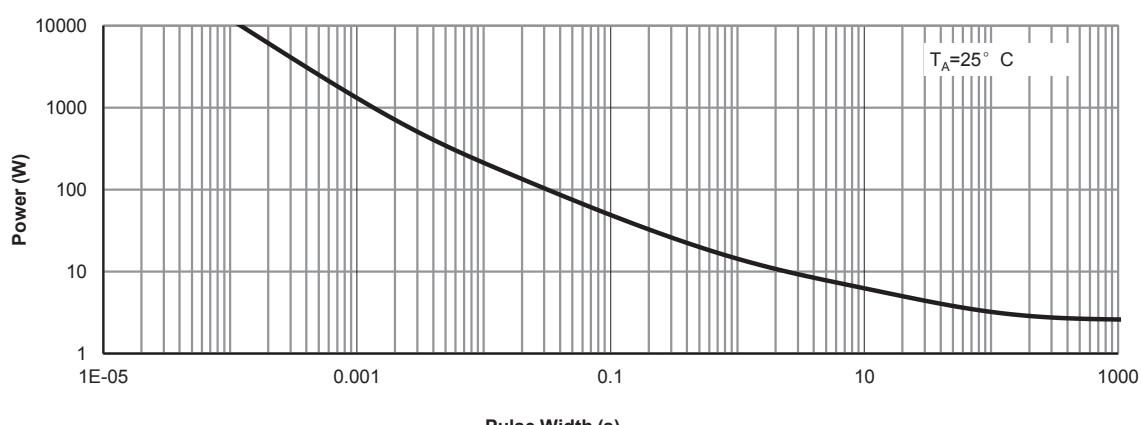


Figure 14: Single Pulse Power Rating Junction-to-Ambient (NOTE 8)

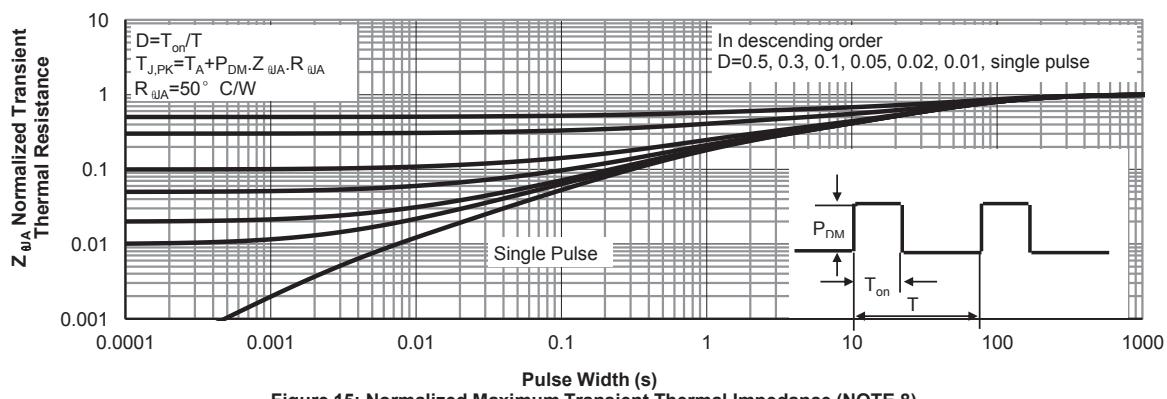


Figure 15: Normalized Maximum Transient Thermal Impedance (NOTE 8)

Figure A: Gate Charge Test Circuit & Waveforms

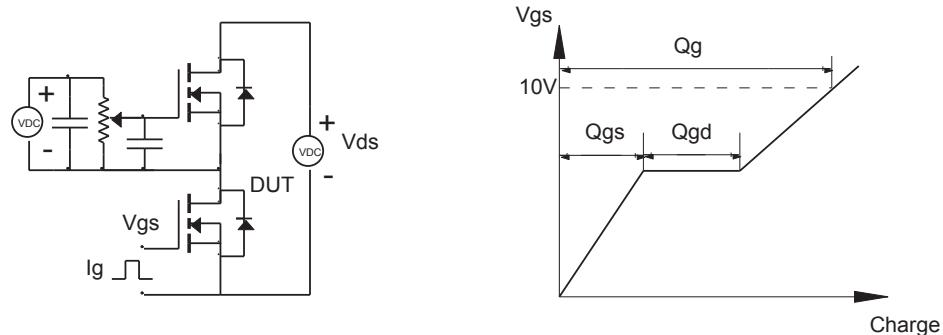


Figure B: Resistive Switching Test Circuit & Waveforms

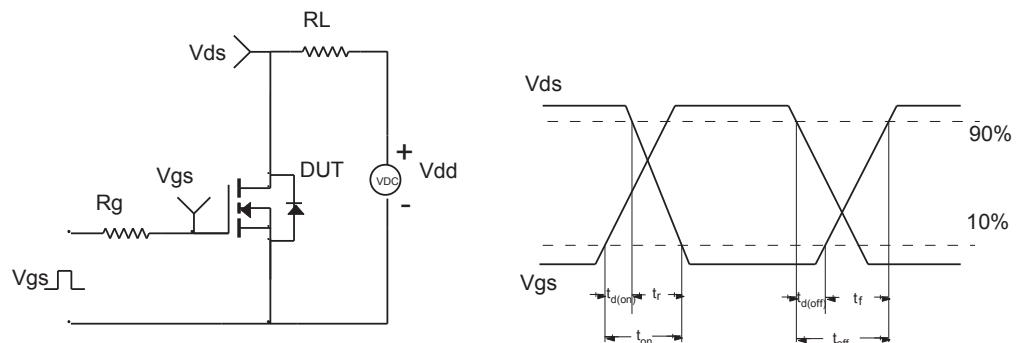


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

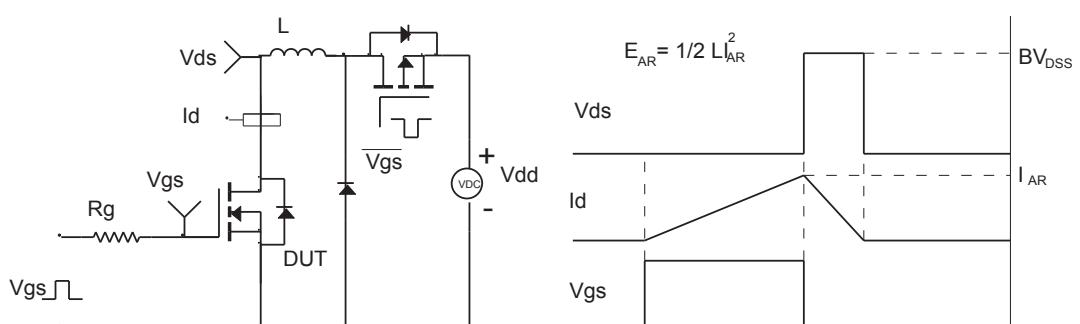
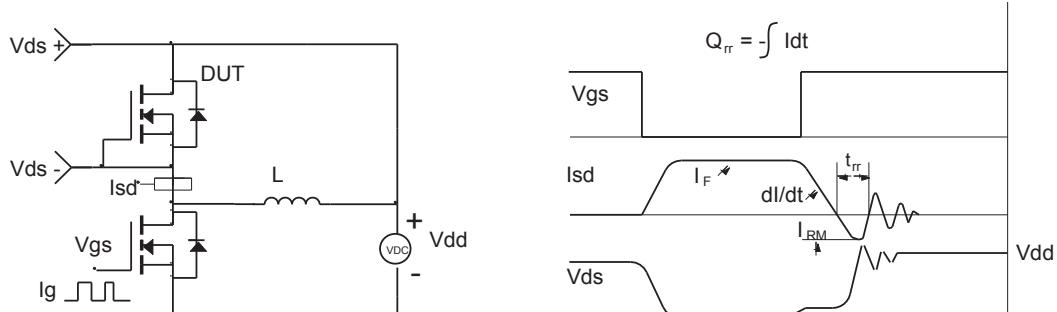
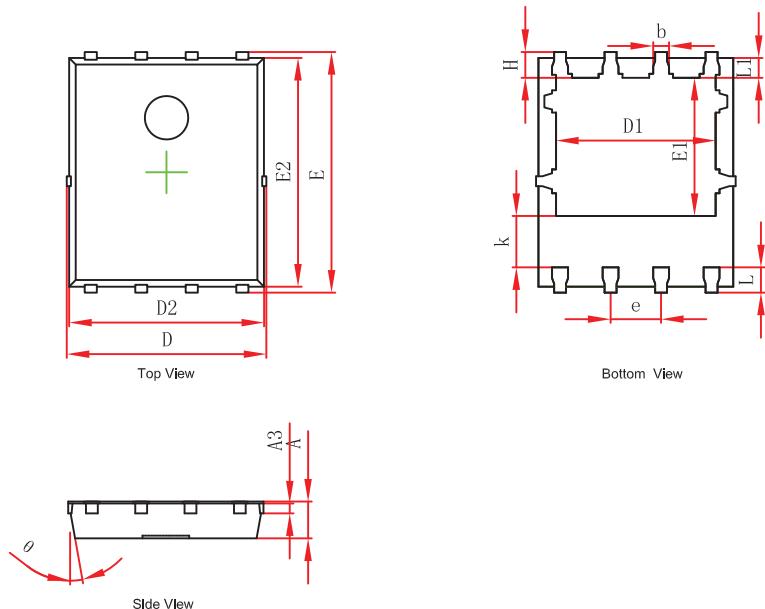
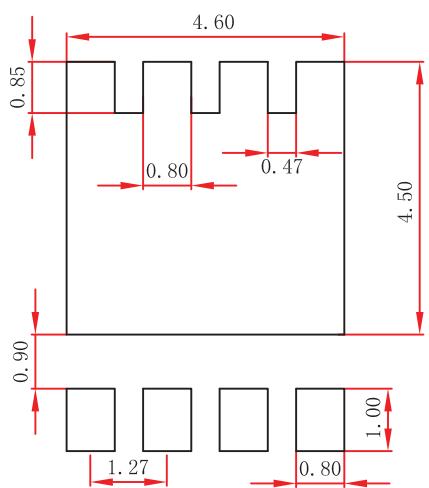


Figure D: Diode Recovery Test Circuit & Waveforms



■ PDFN5x6-8(PDFNWB5x6-8L) Package Outline Dimensions**■ PDFN5x6-8(PDFNWB5x6-8L) Suggested Pad Layout****Note:**

1. Controlling dimension:in millimeters.
- 2.General tolerance: $\pm 0.05\text{mm}$.
- 3.The pad layout is for reference purposes only.